first height is substantially the same as, or greater than, the second height, and said second height is greater than the third height.

22. The semiconductor structure of claim **18** wherein said high-k gate dielectric comprises one of TiO_2, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, La_2O_3, a perovskite-type oxide, and a silicate or nitride thereof.

23. The semiconductor structure of claim **18** wherein said metal-containing gate conductor is one of a conductive metal, an alloy of a conductive metal, a silicide of a conductive metal and a nitride of a conductive metal.

24. The semiconductor structure of claim **18** wherein said high-k gate dielectric at said gate corners has increased bonding as compared to said high-k gate dielectric that is located directly beneath said metal-containing gate conductor.

25. A method of forming a semiconductor structure comprising:

providing a structure including a sacrificial gate and a gate dielectric located on a semiconductor substrate, said structure further including an interlevel dielectric located on said semiconductor substrate and separated from said sacrificial gate by a sacrificial spacer;

removing the sacrificial gate and a portion of the gate dielectric that is not protected by the sacrificial spacer to form an opening that exposes a surface of the semiconductor substrate;

forming a U-shaped high-k gate dielectric and a metal-containing gate conductor inside the opening;

removing the sacrificial spacer to expose a portion of the U-shaped high-k gate dielectric that laterally abuts sidewalls of the metal-containing gate conductor;

removing substantially all of the exposed portion of the high-k gate dielectric that laterally abuts the sidewalls of the metal-containing gate conductor from the gate sidewalls; and

forming a gate spacer in an area that previously included the sacrificial spacer and a portion of the U-shaped high-k gate dielectric.

26. The method of claim **25** further comprising forming an interlevel dielectric material having conductively filled contact vias that extend to the surface of the semiconductor substrate which includes source and drain regions of the at least one MOSFET.

27. The method of claim **26** further comprising forming a spacer liner between the gate spacer and the interlevel dielectric material, the metal-containing gate conductor and the upper surface of both the gate dielectric and the high-k gate dielectric that is present at gate corners of said metal-containing gate conductor.

28. The method of claim **26** further comprising strengthening a portion of said high-k gate dielectric located at gate corners of said metal-containing gate conductor to increase bonding therein as compared to said high-k gate dielectric that is located directly beneath said metal-containing gate conductor.

29. The method of claim **28** wherein said strengthening is obtained by ion implantation one of oxygen ions and nitrogen ions or by a thermal process.

30. The method of claim **26** wherein said forming said gate spacer includes forming a void within in an interior region of said gate spacer.

* * * * *